REMARKS

Present Status of the Application

Upon entry of the amendments in this response, claims 1-11 are pending of which claims 1, 3- 4, 6-7, and 9-10 have been amended without prejudice or disclaimer in order to more explicitly describe the claimed invention. In addition, some errors occur in Fig.3, and thus the Fig.3 was amended as instructed by the examiner. Moreover, enclosed is an amended copy of the specification, of which all informalities and inconsistencies between the specification and the amended claims are corrected. Most importantly, it is believed that no new matter is added by way of amendments made to the claims and the specification. For at least the foregoing reason, applicants respectfully submit that claims 1-11 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion for objection to claims under 35 USC 112,1st and 2nd paragraphs

9. Claims 1-11 are rejected under 35 USC 112,1st paragraph, as containing subject matter which was not described in the specification in such a way to reasonably convey to one skilled in the art had possession of the claimed invention.

12. Claims 1-11 are rejected under 35 USC 112, 2nd paragraph, as being non-operational.

In response thereto, applicants appreciate that the examiner pointed out all the questions pertinent to non-enablement of the claims, which was partly caused by improper literal

translation and others caused by vague technology description. Therefore, all the claims except claims 8 and 11 have been amended without introducing any new matter in order to more precisely clarify the claimed invention. The amended claims are believed to overcome all the questions pertinent to non-enablement of the claims raised by the examiner, as described as follows.

9.1 In re claim 1, an amended phrase of "~~initializing~~ initiating the counting by the instruction counter" can overcome the examiner's questing why the initializing the counting by the instruction counter has to be done when the microprocessor is in the normal operating mode. This is because the word of "initializing" is amended to be "initiating" that means that instruction counter starts to count, instead of being reset to zero as interpreted by the word of "initializing."

As stated in the amended claim 1, in fact, a first upper value and a second upper value are chosen according users' need, and these values are set into the instruction counter and cycle counter respectively when the microprocessor is in the circuit emulation mode.

As to the examiner's question that the values read from the counter at step 4 cannot be used to evaluate the performance because of the two counters' failure to start to count concurrently, as stated in page 11, lines 1-2 in the office action, the step 4 in the amended claim 1 can overcome the preceding examiner's question by being added the sentence of "the instruction counter and the cycle counter start to count concurrently."

As to the examiner's question that how can the program be executed to a definite point, if the microprocessor is in the emulation mode and when the definite point is in the program set, applicants delete the last sentence of "the value inside the instruction counter and the cycle

counter is read to evaluate execution performance and then the microprocessor is triggered into the circuit emulation mode again" in the step 4 and step 5, as well as replace the term of "a definite point" with "an assessment point" so that when the program is executed, the microprocessor is in the normal operating mode and then jumps into the emulation mode if the program is executed to the assessment point.

As to examiner's question that when is the definite point in the program set, in the amended claim 3, its first step definitely described that an assessment point is set up into a breaking register that always exists in the conventional CPU where performance measurement is required when the microprocessor is in the circuit emulation mode. Hence, this first step can answer the examiner's question.

9.2 The examiner questioned that in re claim3, why the initialization of the instruction counter and the cycle counter are not done as the claim 1, as mentioned in the foregoing, the word of "initialization" is amended to be "initiation" in the amended the claim 3. In response to the examiner question, applicants amended the claim 3 to be added by the initiation of the instruction counter and the cycle counter.

9.3 As to the examiner's question that in re claim 6, the specification fails to describe how the upper limits of the instruction counter and the cycle counter are selected, in paragraph [0018], lines 6-7, in the amended specification, there is added to describe these upper values of two counter are chosen according to users' need.

As to the examiner's question that the values read from the counters at elements 2 and 3 cannot be used to evaluate the performance because of the two counters' failure to start to count concurrently, as stated in page 12, line 21-page 13, line 2, in the office action, the step 2 in

the amended claim 6 can overcome the preceding examiner's question by being added the sentence of "the instruction counter and the cycle counter start to count concurrently."

9.4 As to the examiner's question that in re claim 7, the performance of the microprocessor cannot evaluated by using the values either in the instruction counter or in the cycle counter, actually, the performance of the microprocessor must be evaluated by using these two counters and applicants accordingly amended the step 4 in the claim 7 to be the step 5 in the amended claim 7. In addition, the step 5 in the amended claim 7 further describes that the microprocessor is triggered into the circuit emulation mode when either the instruction counter reaches the first upper value or the cycle counter reaches the second upper value.

In addition, in the amended claim 7, a step of "setting a first upper value in an instruction counter and a second value in a cycle counter" is added after the step of "triggering the microprocessor into the circuit emulation mode" in order to overcome the examiner's questioning when two upper values are loaded.

As to the examiner's question how can the program be executed to a definite point, if the microprocessor is in the emulation mode and when the definite point is in the program set, since these questions are the same as the fourth paragraph in "9.1 section," their answer are described.

Furthermore the preceding applicants' response also applies to the examiner's rejections stated in the 12.1-12.5, pages 20-25, under 35 U.S.C. 112, 2nd paragraph because those examiner's rejections are the same as stated in the 9.1-9.5, and applies to the examiner's rejections stated in the 10.1-10.5 as well.

Discussion for objection to claims under 35 U.S.C.103 (a)

16. Claims 1, 6 and 7 are rejected under 35 U.S.C.103 (a) as being untantable over Berc et al.(U.S. Patent 6,112,317) in view of Killian et al. (U.S. Patent 6,477,683).

In response thereto, applicants respectfully tranverse the objection based on the following arguments and thus withdrawal of objections to the claims 1, 6 and 7 is respectfully requested. First of all, Berc discloses a processor performance counter for determining a performance of each instruction. However, Killian (title" Automated Processor Generation System for Design a Configurable Processor And Method for The Same) provide a system which can optimize the hardware implementation and software tools for various performance criteria. Since objectives of Berc are different than those of Killian, there is no motive for any one skilled in the art to combine Berc and Killian to arrive at the subject matter of the amended claim 1, 6 and 7. As a result, Berc and Killian fail to meet the first requirement (i.e. there must be disclosed a teaching, suggesting or motive for combination) for establishing a prima facie case of obviousness.

Furthermore, to establishing a prima facie case of obviousness, the cited references must disclose all limitations of the amended claims 1, 6 and 7. In addition, from col. 13, lines 19-23 in Killian, a debug mode functions to access the internal, software-visible state of the processor, which is distinct from "a circuit emulation mode" as claimed in the amended claims 1, 6 and 7. Moreover, the combination of Berc and Killian still fail to teach, suggest or disclose" setting a first upper value in an instruction counter and a second value in a cycle counter when the microprocessor is in the circuit emulation mode, and the microprocessor is triggered into the

circuit emulation mode when either the instruction counter reaches the first upper value or the cycle counter reaches the second upper value." as claimed in the amended claims 1, 6 and 7. Also, the combination of Berc and Killian still fail to teach, suggest or disclose" triggering the microprocessor into the circuit emulation mode when the program is executed to an assessment point." as claimed in the amended claims 1, 6 and 7. In other words, the combination of Berc and Killian still fail to teach, suggest or disclose" the microprocessor jumps from the normal operating mode into the circuit emulation mode in case of the instructor counter's counting to its preset first upper value, the cycle counter's counting to its preset second upper value or the breaking register's monitoring the program is executed to a preset assessment point, as claimed in the amended claims 1, 6 and 7. Besides, the combination of Berc and Killian still fail to teach, suggest or disclose "setting an assessment point into a breaking register when the microprocessor is in the circuit emulation mode" as claimed in the amended claim 7. As a result, the amended claims 1, 6 and 7 are not obvious over Berc in view of Killian; that is, the amended claims 1, 6 and 7 are patentable under 35 U.S.C. 103 (a).

17. Claims 2 and 8 are rejected are rejected under 35 U.S.C.103 (a) as being untantable over Berc et al.(U.S. Patent 6,112,317) in view of Killian et al. (U.S. Patent 6,477,683), and further in view of Doing et al. (U.S. Patent 6,018,759).

In response thereto, applicants respectfully tranverse the objection based on the following arguments and thus withdrawal of objections to the claims 2 and 8 is respectfully requested. First of all, Doing (titled "Thread Switch Tuning Tool for Optimal Performance in a Computer Processor) functions to provide an improved data processing system and method for

multithreaded processor embodied in the hardware of the processor, and fails to mention the instruction counter's preset first upper value and the cycle counter's preset second upper value as disclosed in the amended claims 1,6and 7. Therefore, the combination of Berc, Killian and Doing still fail to teach , suggest or disclose" triggering the microprocessor into the circuit emulation mode on complete execution of the program" as claimed in the claims 2 and 8. In addition, the claims 2 and 8 are dependent claims so as to contain their respective base independent claims 1and 7. As disused in the preceding section, the combination of Berc and Killian still fail to teach, suggest or disclose" the microprocessor jumps from the normal operating mode into the circuit emulation mode in case of the instructor counter's counting to its preset first upper value, the cycle counter's counting to its preset second upper value or the breaking register's monitoring the program is executed to a preset assessment point, as claimed in the amended claims 1, 6 and 7. Even this combination incorporating Doing, it still fails to make the preceding features of the amended claims 1, 6 and 7 obvious. Hence, claims 2 and 8 are patentable over Berc, in view of Killian and further in view of Doing.

In re claims 3, 4, 9 and 10, the subject matters of theses claims are to "setting up an assessment point into a breaking register where performance measurement is required when the microprocessor is in the circuit emulation mode" as claimed in the amended claims 3, 4, 9 and 10. The examiner further cited Roth (US Publication No. 2002/0078329) as reference for rejecting the claim 4, as it allows extracting state information from the processor pipeline and providing the state information to a control unit for event controlling. However, Roth only extracting state information from the processor, instead of stating when and how to set up an assessment point, as disclosed in the amended claims 3, 4, 9 and 10. Therefore, as none of Berc, Killian , Doing

and Roth teaches, suggests, or discloses any features of the amended claims 3, 4, 9 and 10, as mentioned in the preceding sentence, these amended claims 3, 4, 9 and 10 are not obvious over Berc, in view of Killian and further in view of Doing and Roth. That is, the amended claims 3, 4, 9 and 10 are patentable under 35 U.S.C.103 (a).

As to the claims 5 and 11, even if subject matter of these claims, "the evaluation of microprocessor performance includes: dividing the value inside cycle counter by the value inside the instruction counter," is conventional, they are patentable as a matter of law for at least the reason that they contain all limitations of their base independent claims 1 and 7, respectively, as explained in the preceding paragraph. Hence, the claims 5 and 11 are patentable under 35 U.S.C.103 (a).

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-11 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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In the Drawings:

Applicants appreciates that the examiner pointed out some errors occurred in the Fig.3 so that the Fig.3 was amended as instructed by the examiner. In addition, the amended Fig.3 is believed to be correct.

Annotated Marked-up drawing

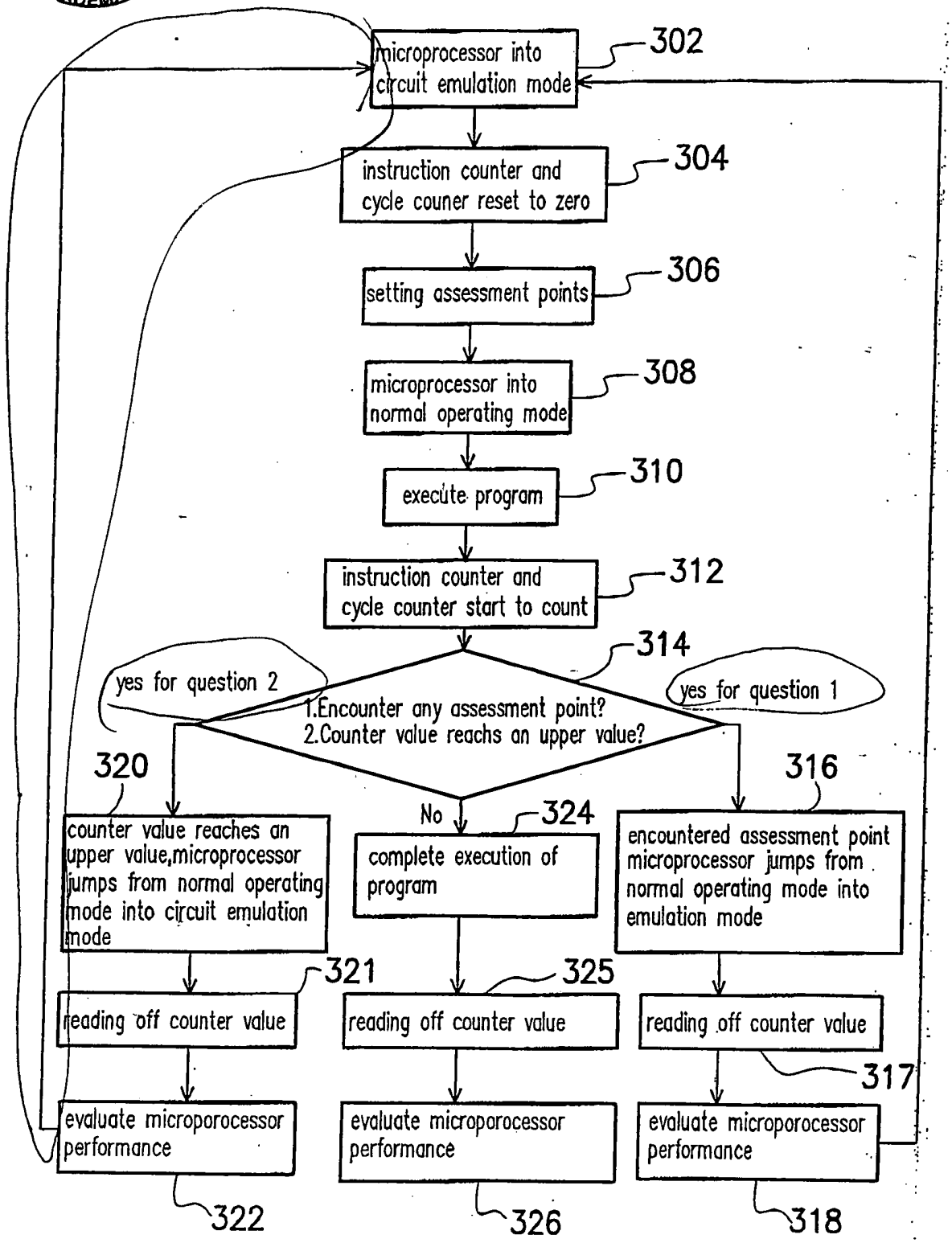

FIG. 3